Please amend the claims as follows:

Sub B4 A1 8. (amended) A low profile, high power semiconductor device including a plastic tape having first and second surfaces, comprising:

a plurality of electrically conductive routing lines and a plurality of contact lands on said first surface, said lands exposed by first openings in said tape;

second openings in said tape configured to accommodate integrated circuit chips;

a chip mount pad in each of said second openings, attached to said first surface and shaped to be coplanar with said second surface;

a circuit chip mounted by means of a thermally conductive material on each of said chip mount pads;

bonding wires connecting said chip to said contact lands;

encapsulating material surrounding said first tape surface including each of said mounted chips and said wire bonds; and

solder balls attached to each of said exposed lands.

A2 11. (amended) The semiconductor device according to Claim 8 wherein said device is created by a transfer molding process of molding compounds, thereby providing mechanical rigidity to said device even when the device thickness is kept to a low profile.

Please add the following new claims:

Sub B5 A3 18. (new) A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal

Sub B5

in said opening such that said portion of said sheet of metal in said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal in said opening having first and second opposing surfaces, said second surface of said sheet of metal in said opening being coplanar with said second surface of said substrate;

an integrated circuit chip mounted on said first surface of said sheet of metal in said opening.

A3

19. (new) The packaged integrated circuit of Claim 18, further comprising encapsulant covering at least a portion of said first surface of said substrate and said chip, wherein said encapsulant does not cover said second surface of said substrate and does not cover said portion of said sheet of metal in said opening coplanar with said second surface of said substrate.

20. (new) The packaged integrated circuit of Claim 18, further comprising a heatsink attached to said second surface of said sheet of metal in said opening.

21. (new) The packaged integrated circuit of Claim 18, wherein said second surface of said sheet of metal in said opening is attached to a printed circuit board.

22. (new) A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad;

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encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, but does not cover said bottom surface of said chip mount pad.

23. (new) The packaged integrated circuit of Claim 22, further comprising a heatsink attached to said bottom surface of said chip mount pad.

24. (new) The packaged integrated circuit of Claim 22, wherein said bottom surface of said chip mount pad is attached to a printed circuit board.

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A3

25. (new) A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface, said opening having a first size;

a plurality of contact lands on said first surface of said substrate adjacent to said opening;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad, said integrated circuit chip having a second size, wherein said second size is smaller than said first size;

bond wires coupling said integrated circuit chip to said contact lands; and

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, bond wires, and contact lands, but does not cover said bottom surface of said chip mount pad.

26. (new) The packaged integrated circuit of Claim 25, wherein said substrate is plastic tape.